This listing of claims replaces all prior versions, and listings of claims in the instant application:

Listing of Claims:

1.   (Original) An integrated circuit comprising:

a plurality of memory arrays;

Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, wherein the ASI bus interface logic controls access to the plurality of memory arrays;

a memory control unit connected to the ASI bus interface logic; and

a memory built-in self-test (MBIST) engine connected to the ASI bus interface logic, wherein the MBIST engine utilizes the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays.

2.   (Original) The integrated circuit as defined in claim 1, wherein the MBIST engine further comprises:

a programmable state machine controller;

a programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation;

a programmable address generator connected to the controller, wherein the address generator provides addresses appropriate for the particular test situation; and

a programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller.

3.   (Original) The integrated circuit as defined in claim 2, wherein the MBIST engine further comprises a storage connected to the controller, wherein the storage contains information for the controller.

4.   (Original) The integrated circuit as defined in claim 1, wherein the MBIST engine generates a test output as a product of the memory testing.

5.   (Original) The integrated circuit as defined in claim 4, wherein the MBIST engine institutes an action as a product of the memory testing.

6.   (Original) The integrated circuit as defined in claim 1, wherein the MBIST engine institutes an action as a product of the memory testing.

7.   (Original) A memory built-in self-test (MBIST) engine for an integrated circuit having a plurality of memory arrays, Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, and a memory control unit connected to the ASI bus interface logic, wherein the MBIST engine utilizes the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays, the MBIST engine comprising:

a programmable state machine controller;

a programmable data generator connected to the controller, wherein the data generator provides data appropriate for a particular test situation;

a programmable address generator connected to the controller, wherein the address generator provides addresses appropriate for the particular test situation; and

a programmable comparator connected to the controller, wherein the comparator provides test results information for the particular test situation to the controller.

8.   (Original) The MBIST engine as defined in claim 7, further comprising a storage connected to the controller, wherein the storage contains information for the controller.

9. (Original) The MBIST engine as defined in claim 7, wherein the MBIST engine generates a test output as a product of the memory testing.

10. (Original) The MBIST engine as defined in claim 9, wherein the MBIST engine institutes an action as a product of the memory testing.

11. (Original) The MBIST engine as defined in claim 7, wherein the MBIST engine institutes an action as a product of the memory testing.

12. (Original) A method of memory built-in self-test (MBIST) for an integrated circuit having a plurality of memory arrays, Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, a memory control unit connected to the ASI bus interface logic, and an MBIST engine connected to the ASI bus interface logic, the method comprising:

utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays.

13. (Original) The method as defined in claim 12, further comprising generating a test output as a product of the memory testing.

14.   (Original) The method as defined in claim 13, further comprising instituting an action as a product of the memory testing.

15.   (Original) The method as defined in claim 12, further comprising instituting an action as a product of the memory testing.

16.   (Original) An apparatus for memory built-in self-test (MBIST) for an integrated circuit having a plurality of memory arrays, Address Space Identifier (ASI) bus interface logic connected by an ASI bus to the plurality of memory arrays, a memory control unit connected to the ASI bus interface logic, and an MBIST engine connected to the ASI bus interface logic, the apparatus comprising:

means for utilizing the ASI bus interface logic to perform memory testing on at least one of the plurality of memory arrays.

17.   (Original) The apparatus as defined in claim 16, further comprising means for generating a test output as a product of the memory testing.

18. (Currently Amended) The apparatus as defined in claim
~~18~~ 16, further comprising means for instituting an action as a
product of the memory testing.

19. (Original) The apparatus as defined in claim 16, further
comprising means for instituting an action as a product of the
memory testing.